More on Analog Decoupling for Microcontrollers

Inspired By:
The Right Way to Use LC Filters on Microcontroller Analog Interfaces

https://www.youtube.com/watch?v=mSehCGvPXOI&ab_channel=AltiumAcademy

Hey Zach !

I **LOVE** your videos and have been an Altium customer for about 14 years.

Upfront I want to say that you did an excellent presentation but I really want to expand on a couple of ideas backed up by "reasonable but not perfect simulations".

STEP 1: Replicate your simulation results (I use LTSpice but that does not matter at all you can use Altium, LTSpice, QSpice, TI Tina, Whatever). I took out the capacitors on VREG side because in simulation life they do nothing along with C1 since the VREG can supply any required current at any required switching rate (love ideal voltage sources). Used an ideal switch instead of an NMOS FET.

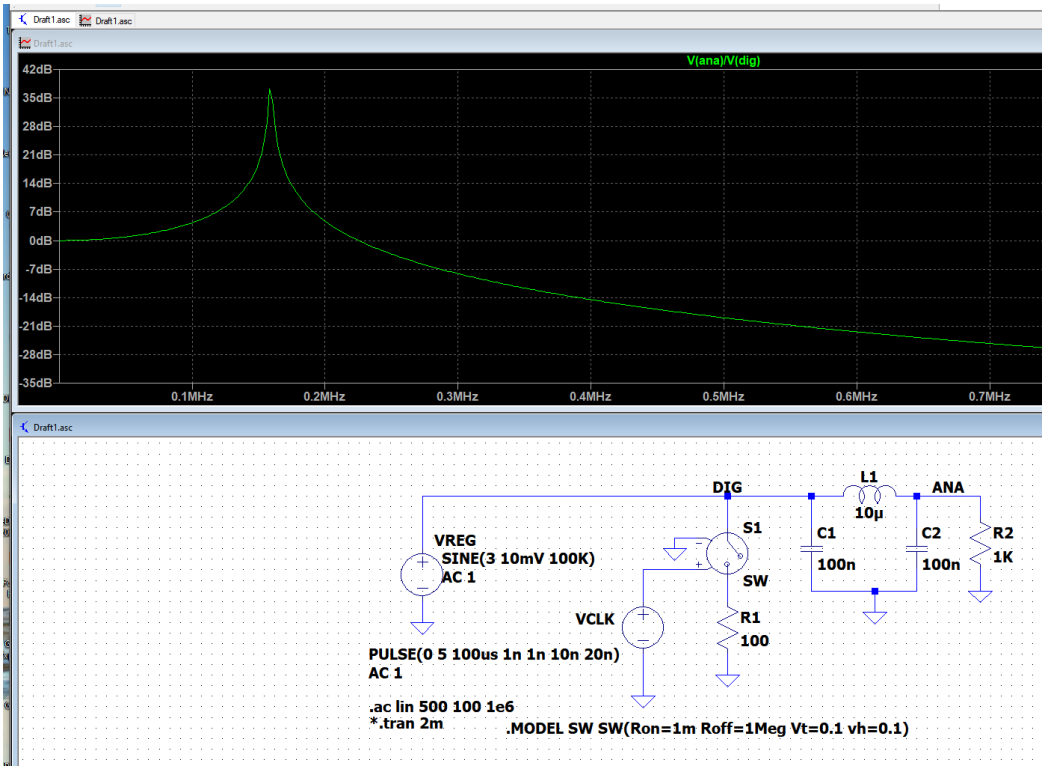


Figure 1: Zach's Demonstration Model + AC Analysis (Shows same resonant frequency)

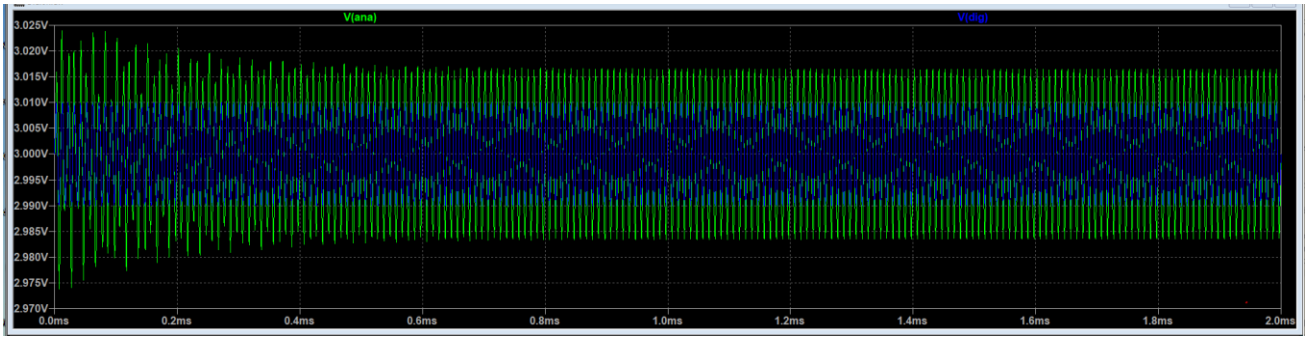


Figure 2: Transient Analysis showing voltage increase on analog rail (bad times)

Okay this looks about the same as the video.

Let's Make The "Load" More Realistic

STM32G431 (operating at 50MHz)(See VCLK)(2xADCs and 4xDACs)

Power Supply Recommendations from ST Microelectronics

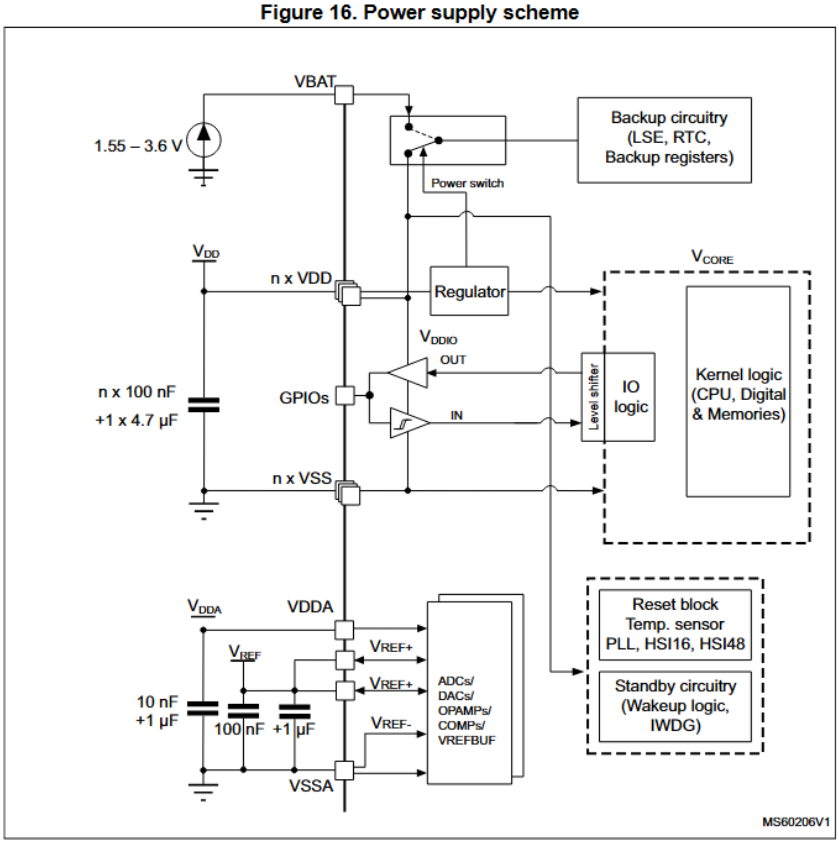
The STM32G431x6/x8/xB devices require a 1.71 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies, can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V
  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.
- V_{DDA} = 1.62 V to 3.6 V (see *Section 5: Electrical characteristics* for the minimum V_{DDA} voltage required for ADC, DAC, COMP, OPAMP, VREFBUF operation).
  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage and should preferably be connected to V_{DD} when these peripherals are not used.

Figure 3: ST Microelectronics Power Requirements

5.1.6 Power supply scheme

Figure 16. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Figure 4: Recommended Decoupling Scheme (implied split supply)

I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 4 Msps	-	590	730	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 4 Msps	-	110	140	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 4 Msps	-	220	270	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design.

Figure 5: Worst Case ADC Current Requirements

I_{DDA}(DAC)	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x Ton/(Ton +Toff) (4)	670 x Ton/(Ton +Toff) (4)	

Figure 6: DAC Worst Case Power 670uA (x4)

Now let's make ourselves a bit more of a realistic analog model by switching the analog current along with a static power draw. Say we are using 2 ADCs and 4 DACs plus some overhead.

Totaling everything up: 2 x 730uA (adcs) + 4 x 670uA (dacs) = 4140uA = 4.14mA

Let's assume 10mA just to give us overhead and in-case life happens and Murphy's Law applies.

Here is a "better" model (2 ADCs switched at 4MHz & 2mA, 8mA static draw).

Model the static and dynamic current with ideal current sources.

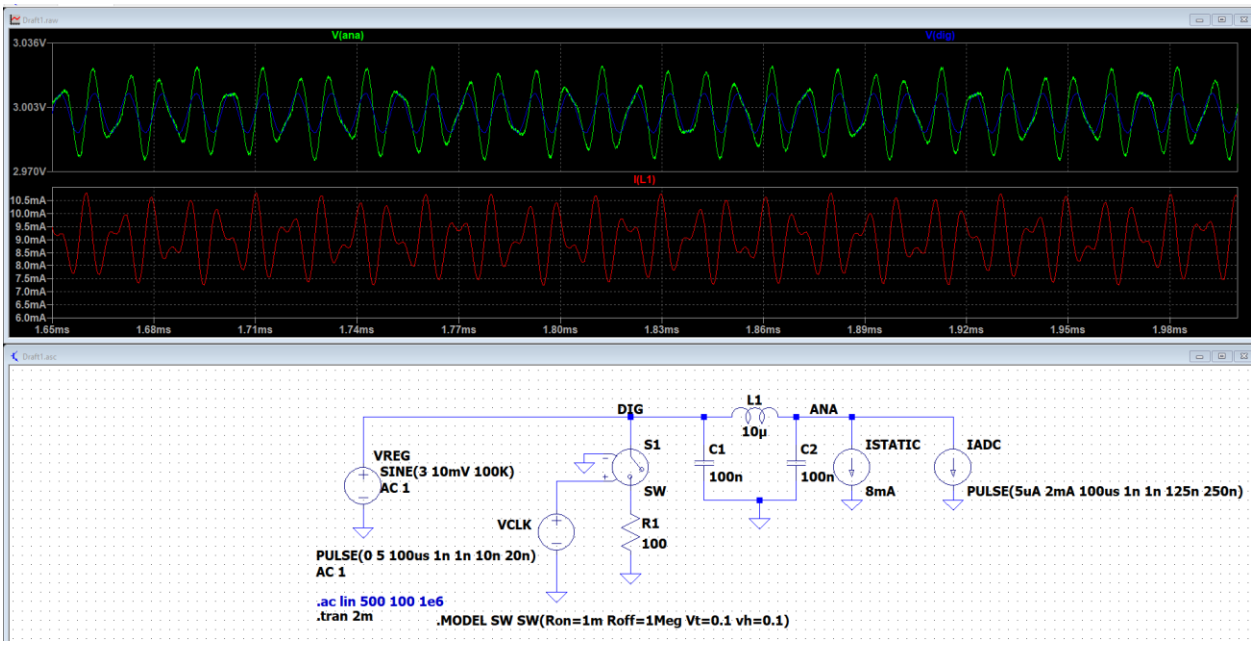


Figure 7: Zach's Model with Dynamic + Static Switching – has more peak to peak noise

Now this is WORSE than the first model → **GREAT** we are on the right track.

Let's give this solution a **C-** (it will work for modest analog applications that don't require amazing ENOB and SNR)

Next Step

FOLLOWING STM32 GUIDELINES: 10nF + 1uF on Analog Rail (From Figure 4)

Replace our 100nF capacitor with STM recommended 1uF + 10nF capacitors and let's see what happens.

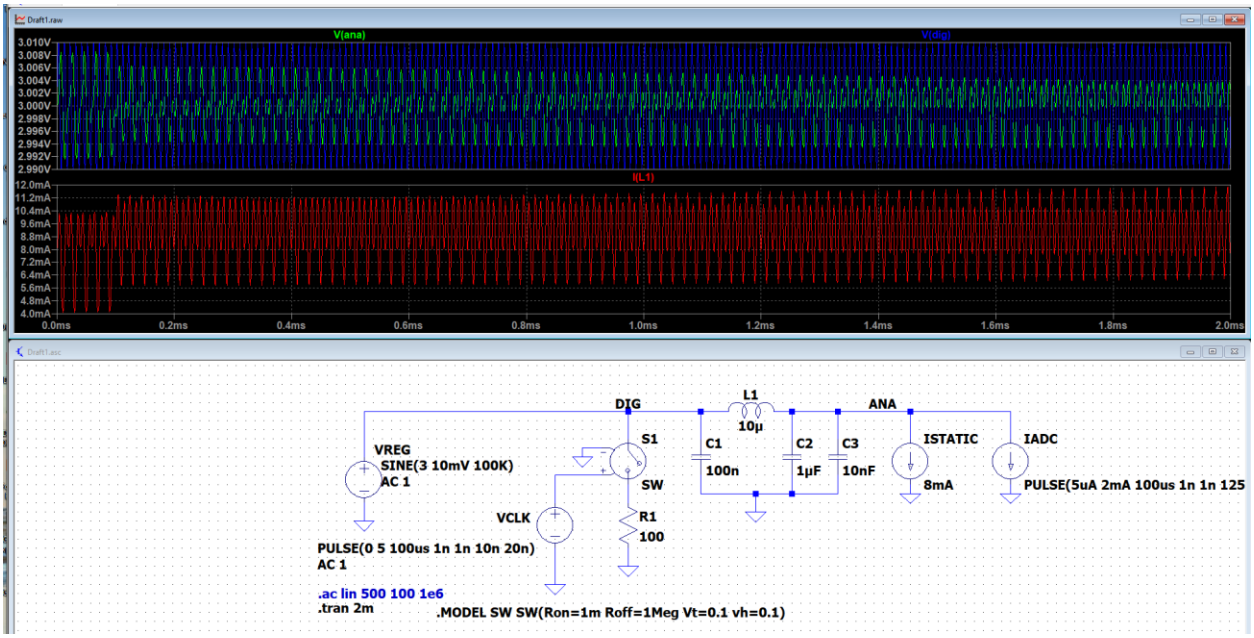


Figure 8: STM Recommended Decoupling

We damped down the noise quite a bit with a much more aggressive decoupling scheme. Intuitively the 1uF capacitor is supply enough current for the DC portion of the switching and the 10nF is supplying current for the AC portion. Both contribute but essentially they "decouple" out the L1 inductor who is now solely responsible for keeping C2 and C3 charged over a longer period. We are probably discharging C2 and C3 a bit too much since the sampling frequency of the ADCs is 4MSPS but still not bad.

Let's give this solution a solid **B.**

<You Can Skip This>

(6mv of rail noise assume PSRR = -40dB)

Noise = Vnoise / sqrt(100Khz,sw) * $10^{(-40/20)}$ = 6mv / 316 * 0.01 = 190nV

SNR = 20*log(Vfullscale/Vnoise) = 20*log(3/190nV) = 144dB

So this is not a big contributor to the performance of your ADC. Other factors are jitter on the sample clock, sample and hold uncertainty and parasitics, input referred noise, reference bounce, injected noise on the silicon from the digital path, noise from coupled digital switching, etc. etc.

</You Can Skip This>

Next Step

NOW LET'S DO EVEN BETTER – REPLACE 1UF WITH 10uF (0402 GMC04X5R106M10NT)

Going with the above theory lets supply A LOT of charge to the analog rail.

We can do this because the Voltage rail is ~3.3V and they are making 10uF capacitors with good parasitics in 0402 packages with a working voltage ~10V these days (good times).

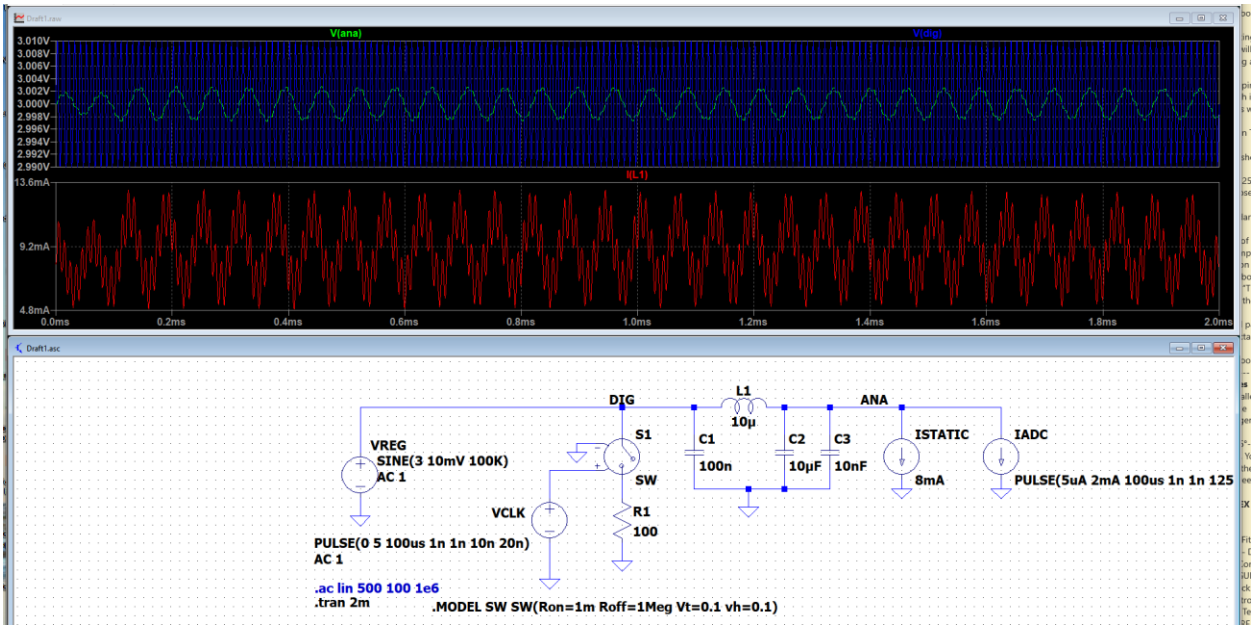


Figure 9: Realistic 10uF Capacitor Simulation ~ 4mv Pk-Pk instead of 6mV

Cheap and easy upgrade with no change in layout.

Let's give this solution a solid **B+.**

Kind of tempted to stop here but nope…..

Next Step

Let's try 2x10uFs and get rid of the 10nF capacitor and change L1 to 1uH (easy to buy in 0402).

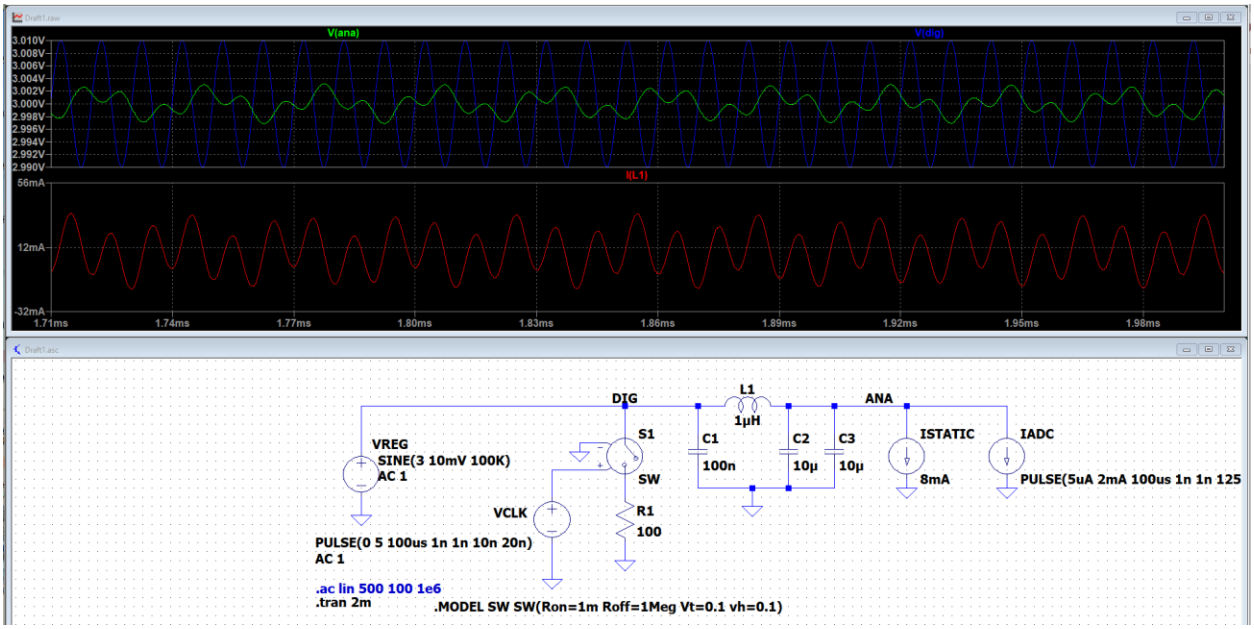


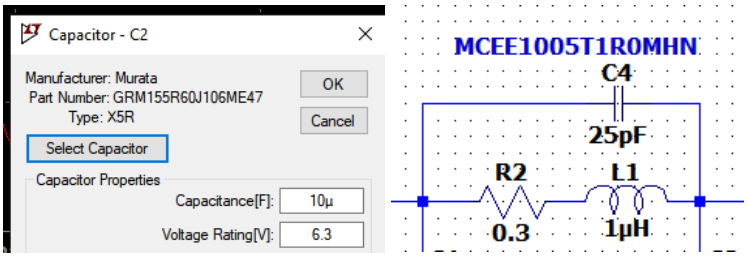
Figure 10: 2x10uF realistic capacitors 4mV pk-pk noise with a smaller 1uH inductor - nice

Cheap and easy upgrade with no change in layout.

Let's give this solution a solid **B+.**

Next Step

CHANGE CAPACITORS C2, C3 and L1 to the below model with "realistic" parasitics.



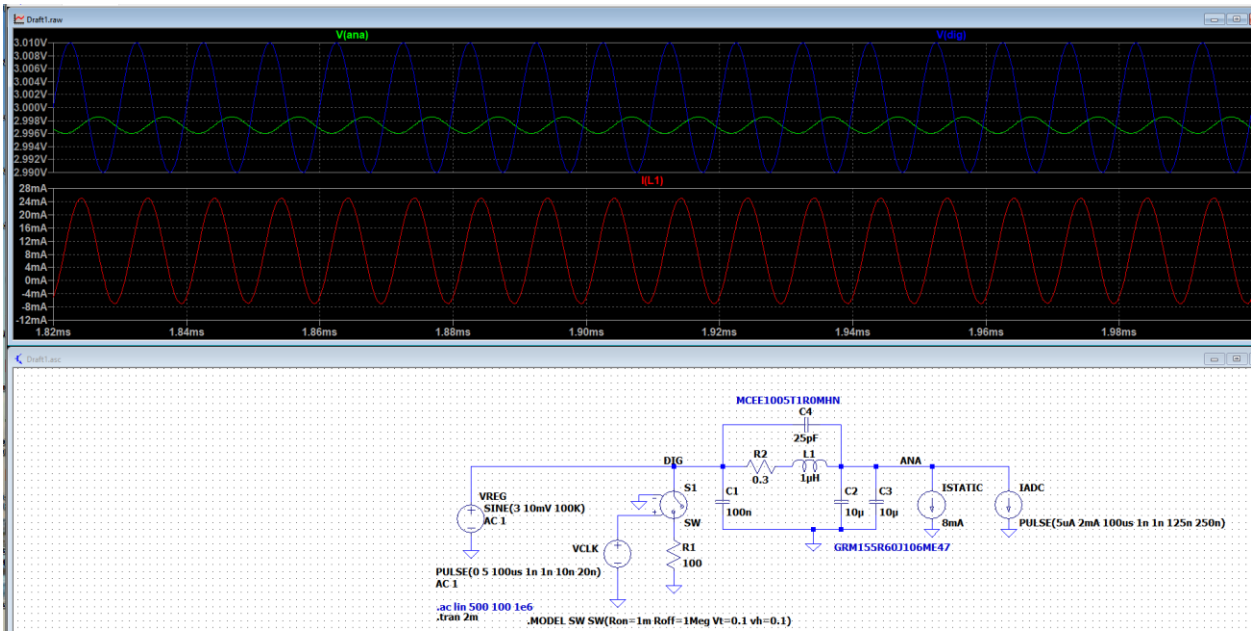


Figure 11: Kind of beautiful 2mV pk-pk noise with a good parasitic model for L and C

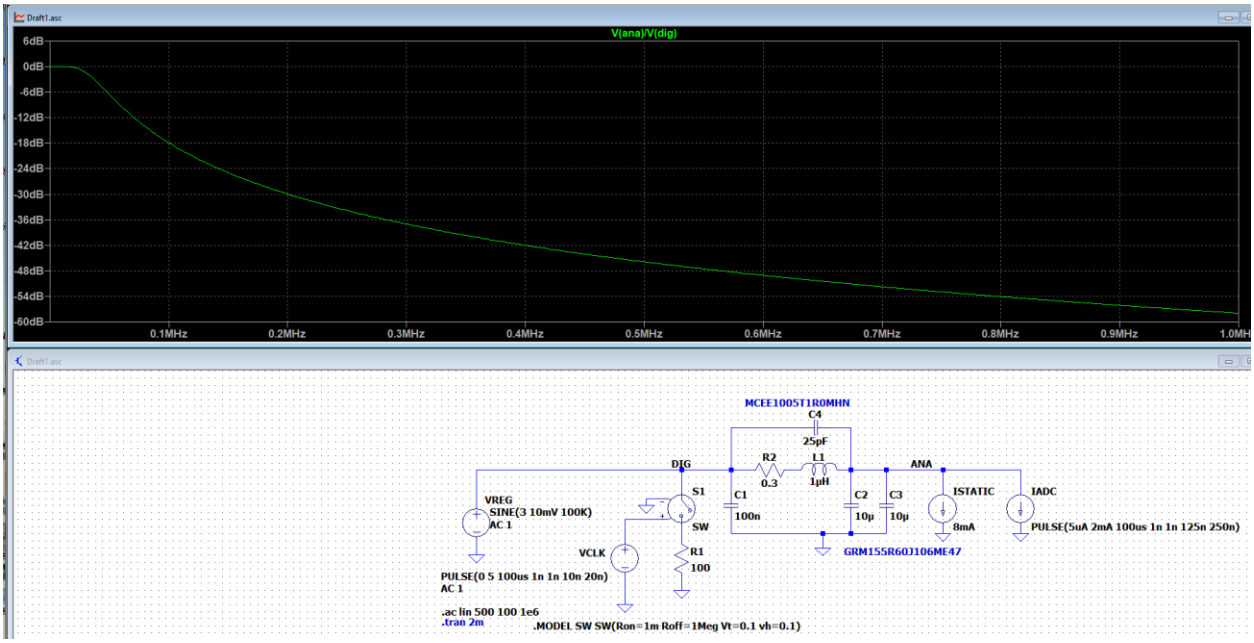


Figure 12: Nice Damped Filter Response – Is our B+ solution actually an A ?

What happened here? Basically, the DCR of the inductor killed resonances at the expense of a little bit of a DC drop for the Analog Rail. All the peaking is gone and the Analog Circuits have plenty of current available from 20uF of decoupling capacitance. I would add in a 10nF capacitor just in case because of the package parastics of the device but that's just me.

Primary Lesson: Chose the biggest capacitors you can in the smallest package you need.

Doubling the capacitors cuts the parasitics (½ ESR + ½ ESL) of the capacitors in exactly the way you want. Place them close to the pins of the part and make sure you have good ground vias. Multiple ground vias cut the inductance which is good even though the total current is small. Bigger capacitors can supply more charge over a longer period of time and parallel them lets them supply that charge less hindered by parasitics. Discharge rate of those capacitors is gated by the package parasitics of your device.

Secondary Lesson:

The cut-off frequency of your PI filter should be 10x less than your switching frequency to allow good attenuation. **BUT** You need enough capacitance on the other side of the filter to supply the dynamic current you need for multiple cycles of the switching frequency of the analog circuits to allow the decoupling capacitors enough time to recharge.

Tertiary Lesson:

Manufacturer recommendations are guidelines that can be modified if you are careful to model your situation properly. Manufacturer recommendations and evaluation boards are designed for the GENERAL use case because the Manufacturer does not know each customers requirements and they try to ship something that will work for most use cases (and show off their brand new shiny silicon).

Final Words:

Is the B+ solution an A ?

Let's let Zach decide.

Personally, nothing is an A because we always have to fix things until they break.

Thank you Zach for all your efforts,

Mike